Linear Integrated Circuits & Pulse and Digital Circuits
LABORATORY MANUAL (EEE-318)
(III/IV EEE Ist Semester)

Prepared By
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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Vision of the Institute

ANITS envisions to emerge as a world-class technical institution whose products represent a good blend of technological excellence and the best of human values.

Mission of the Institute

To train young men and women into competent and confident engineers with excellent communication skills, to face the challenges of future technology changes, by imparting holistic technical education using the best of infrastructure, outstanding technical and teaching expertise and an exemplary work culture, besides molding them into good citizens

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Vision of the Department

To become a centre of excellence in Education, research and produce high quality engineers in the field of Electronics and Communication Engineering to face the challenges of future technological changes.

Mission of the Department

To achieve vision department will

Transform students into valuable resources for industry and society by imparting contemporary technical education.

Develop interpersonal skills and leadership qualities among students by creating an ambience of academic integrity to participate in various professional activities

Create a suitable academic environment to promote research attitude among students.

Program Educational Objectives (PEOs):

PEO1 : Graduates excel in their career in the domains of Electronics, Communication and Information Technology.

PEO2 : Graduates will practice professional ethics and excel in professional career through interpersonal skills and leadership qualities.

PEO3 : Graduates demonstrate passion for competence in higher education, research and participate in various professional activities.

Program Outcomes (POs):

Engineering Graduates will be able to:

1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSOs):

PSO1 **:** Implement Signal & Image Processing techniques using modern tools.

PSO2 **:** Design and analyze Communication systems using emerging techniques.

PSO3 **:** Solve real time problems with expertise in Embedded Systems.

LINEAR IC'S & PULSES & DIGITAL CIRCUITS LABARATORY	
EEE 318	**Credits: 2**
Instruction: 3 Practical's / Week	Sessional Marks: 50M
End Exam: 3 hrs	End Exam Marks: 50M

COURSE OUTCOMES:

1. Analyze and Design various application circuits using op-amp such as summing amplifier, integrator, differentiator and Schmitt trigger
2. Analyze and Design linear wave shaping circuits and non linear wave shaping circuits
3. Analyze and Design Multivibrator circuits using op-amp, Transistor and 555Timer.
4. Design active filters for the given specifications and obtain their frequency response characteristics.
5. Analyze and Design ramp voltage generators by using UJT & Bootstrap circuit.

CO-PO Mapping

Mapping of course outcomes with program outcomes & program specific outcomes:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO9	PO10	PSO1	PSO2	PSO3
CO1	1	1	3	3	1	1	2	1	1	0	1
CO2	1	1	3	1	1	1	2	1	1	0	1
CO3	1	1	3	2	1	1	2	1	1	0	1
CO4	1	1	3	3	1	1	2	1	1	0	1
CO5	1	1	3	1	1	1	2	1	1	0	1

Correlation levels 1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High)

Assessment CO matrix:

Assessment type		Course Outcome				
		CO1	CO2	CO3	CO4	CO5
Record		20%	20%	20%	20%	20%
Internal Lab Exam	Circuit Diagram & Procedure		40%	30%		20%
	Result & Graph			30%	20%	
	Viva	20%			40%	10%

LINEAR IC'S & PULSES & DIGITAL CIRCUITS LABARATORY
LIST OF EXPERIMENTS

Scheme of Evaluation

(LINEAR INTEGRATED CIRCUITS & PULSE AND DIGITAL CIRCUITS LABORATORY)

Internal Marks (50M):

Internal lab Exam	: 25M
Continuous evaluation	: 25 M

Distribution of Continuous evaluation marks:

a) Viva on every lab session	: 5M
b) Observation with final results	: 5M
c) Record	: 10M
d) Attendance	: 5M

Distribution of Record Marks (10M):

a) Aim and apparatus	: 1M
b) Circuit diagrams	: 2M
c) Theory	: 2M
d) Tabular from & calculations	: 2M
e) Procedure with theoretical calculations	: 1M
f) Graph	: 1M
g) Result/Conclusion	: 1M

Internal / External Lab Marks division:

Internal Exam (25 M)		**External Exam (50 M)**	
Write up	: 5M	Write up	:10M
Execution/Performance	: 10M	Execution	:20M
Graphs & Result	: 5M	Graphs & Result	:10M
Viva	: 5M	Viva	:10M

RUBRICS

S.No	Competency	Performance Indicator
1.	Demonstrate an ability to conduct experiments consistent with their level of knowledge and understanding.	Laboratory preparation & finding the appropriate values of the components to meet the specifications (verification of Lab observation)
		Stating clearly the aim of the experiment, its scope and importance for purpose of doing experiment & Oral Presentation (Based on viva)
2.	Demonstrate an ability to design experiments to get the desired output.	Experimental procedures & ability to construct the circuit diagram on a bread board and use meters/ instruments to record the measured data according to the range selected (Based on physical observation)
3.	Demonstrate an ability to analyze the data and reach valid conclusions.	Presentation of record & Conclusions of the lab experiment performed. (Based on Lab record)

S.No	Performance Indicator	Excellent (A) 100%	Good(B) 80%	Need improvement (C) 60%	Fail (D) <40%
1.	Laboratory preparation & ability to construct the circuit diagram on a bread board and use meters/ instruments to record the measured data according to the range selected (Based on physical observation) (5M)	Read and understand the lab manual before coming to lab. Observations are completed with necessary theoretical calculations including the use of units and significant figures & Obtain the correct values of the components after calculations. Follow the given experimental procedures, to obtain the desired output.	Observations are completed with necessary theoretical Calculations but With-out proper understanding & Obtain the correct values for only few components after calculations. Follow the given experimental procedures, but obtained results with some errors.	Observation s are incomplete &Obtain the incorrect values for components. Lacks the appropriate knowledge of the lab procedures. Has no idea what to do	No effort exhibited
2.	Stating clearly the aim of the experiment, its scope and importance for purpose of doing experiment & Oral Presentation (Based on viva)(5M)	Clearly describes the purpose of doing experiment and its scope. Responds confidently, and precisely in giving answers to questions correctly	Clearly describes the purpose of doing experiment. Responds in giving answers to questions but some answers are wrong.	Some idea of doing experiment but not very clear & responds in giving answers to questions but all answers are wrong.	No effort exhibited
3.	Presentation of record & Conclusions of the lab experiment performed. (Based on Lab record)(10M)	Well-organized, interesting, confident presentation of record & able to correlate the theoretical concepts with the concerned lab results with appropriate reasons.	Presentation of record acceptable	Presentation of record lacks clarity and organized	No effort exhibited

About the lab:

In pulse circuits lab students will be able to analyze and design different linear and non-linear waveforms with different time constants and different types of inputs, with and without reference voltages using linear and non-linear wave shaping circuits. Design, analysis and voltage regulators circuits will be done.

In Integrated circuits lab Design and analysis of linear and non-linear circuits using operational amplifiers, 1st & 3rd order active filters, voltage Regulators, Multivibrator using timers, Schmitt trigger circuits will be done. Identification, verification and applications of ICs like LM741, 555 timer and three terminal regulators (7805, 7808 etc.) will be taught. With this knowledge students will be able to do the mini-projects with the help of integrated circuits.

LIST OF MAJOR EQUIPMENT IN EDC-II/LIC&PC LABORATORY

SL.NO	NAME OF THE EQUIPMENT	MAKE	QUANTITY
1.	20 MHz DUAL TRACE OSCILLOSCOPE	AP LAB /SCIENTIFIC	16
2.	1 MHz FUNCTION GENERATOR WITH DIGITAL DISPLAY	AP LAB/ PACIFIC	14
3.	TRPS 0-30V, 2A DUAL CHANNEL ITL	ITL/PACIFIC /FALCON	16
4.	DC MICRO & MILLI AMMETERS	MECO/HI- Q/AQUILA	47
5.	DC MICRO VOLTMETER MECO	MECO/HI- Q/AQUILA	13
6.	BENCH TOP DIGITAL MULTIMETER	METRAVI/ MECO	15
7.	5KVA SERVO CONTROLLED STABILIZER	HI- Q	01

TOTAL EXPENDITURE OF THE LABORATORY (including consumables): Rs. 13,78,942.41/-

EDC-II Laboratory

Do's

1. Be punctual and regular to the laboratory.
2. Maintain Discipline all the time and obey the instructions.
3. Check the connections properly before turning ON the circuit.
4. Turn OFF the circuit immediately if you see any component heating.
5. Dismount all the components and wires before returning the kit.
6. Any failure / break-down of equipment must be reported to the faculty

Don'ts

1. Don't touch live electric wires.
2. Don't turn ON the circuit unless it is completed.
3. Avoid making loose connections.
4. Don't leave the lab without permission.
5. Do not handle any equipment without reading the instructions/Instruction manuals

EXPERIMENT NO: 1

MEASUREMENT OF OP – AMP PARAMETERS & APPLICATIONS

Objective:

a) Measurement of Op – Amp Parameters: To determine the CMRR and slew rate of operational amplifier.

b) Applications of Op – Amp: To realize Summing Amplifier and Subtracting Amplifier by using 741 Op-Amp.

S.No	Apparatus	Type	Range	Quantity
01	Operational Amplifier	LM 741IC		01
02	Resistance		100Ω (2),100KΩ (2) ,10K (1) , 1KΩ (4) 15KΩ(1)	
03	Regulated Power supply		(0-30V)	01
04	DC multimeter,			
05	Signal Generator		1M Hz	01
06	CRO			01
07	Breadboard and Wires ,CRO Probes			

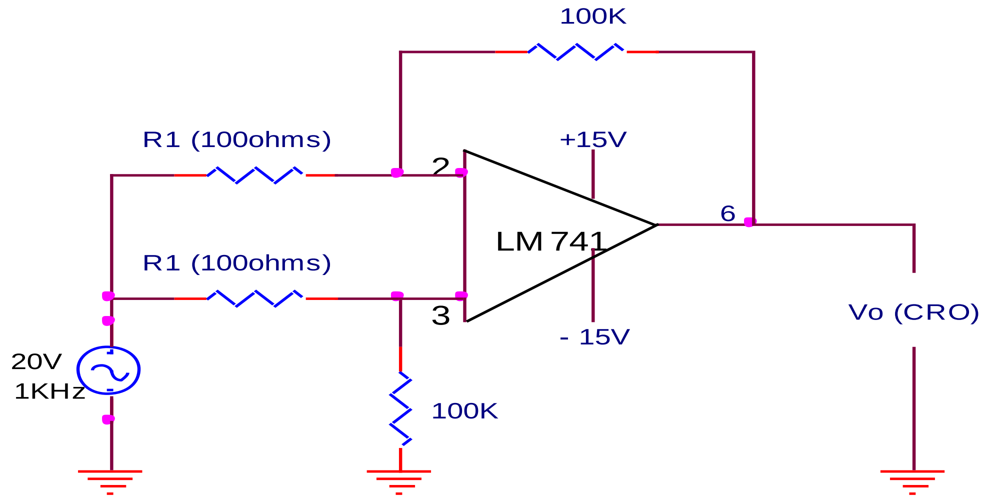
THE IDEAL OP AMP:

An ideal op amp would exhibit the following electrical characteristics.

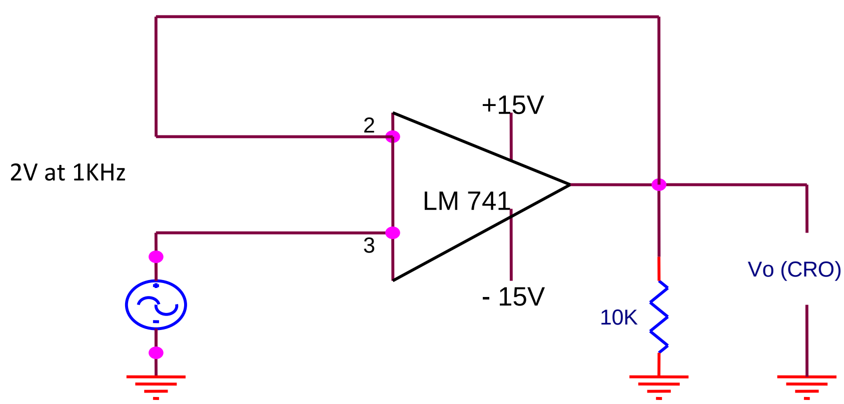
1. Infinite voltage gain A.
2. Infinite input resistance R_i so that almost any signal source can drive it and there is no loading of the preceding stage.
3. Zero output resistance R_0 so that output can drive an infinite number of other devices.
4. Zero output voltage when input voltage is zero.
5. Infinite bandwidth so that any frequency signal from 0 to ∞ Hz can be amplified without attenuation.
6. Infinite common mode rejection ratio so that output common – mode noise voltage is zero.
7. Infinite slew rate so that output voltage changes occur simultaneously with input voltage changes.

CIRCUIT DIAGRAM: a) Measurement of Op – Amp Parameters

1. CALCULATION OF CMRR



2. SLEW RATE:



Procedure:

COMMON MODE REJECTION RATIO:

1. Connections are made as shown in circuit diagram.
2. A DC supply of 15V is given.
3. An input signal of 20V at 1 KHz is given from the signal generator.
4. The output voltage Vo is measured from the CRO is calculated by the formula

CMRR= (1 + RF /R1) (VS /VO)

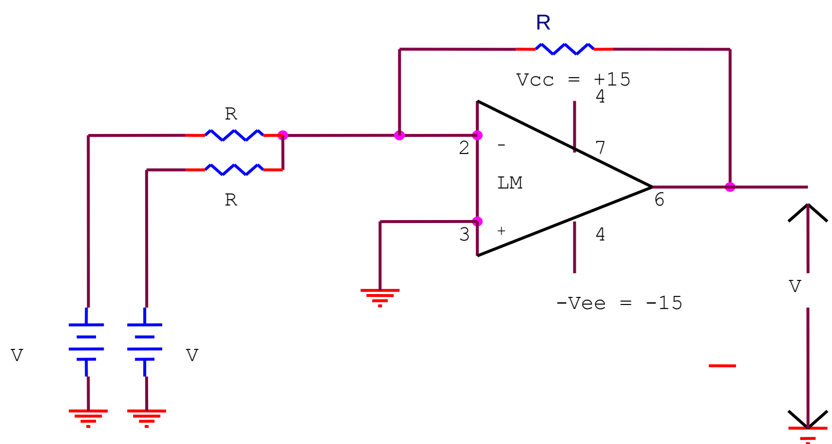
SLEW RATE:

1. Connections are made as shown in circuit
2. A Dc dual supply of 15V is given from the TRPS.
3. An input signal of 2V at 1KHz is given from the signal generator.
4. The frequency is increased gradually and the voltage at which square wave transforms into triangular wave is noted. The value of frequency is also noted.
5. The slew rate is calculated by the formula.,

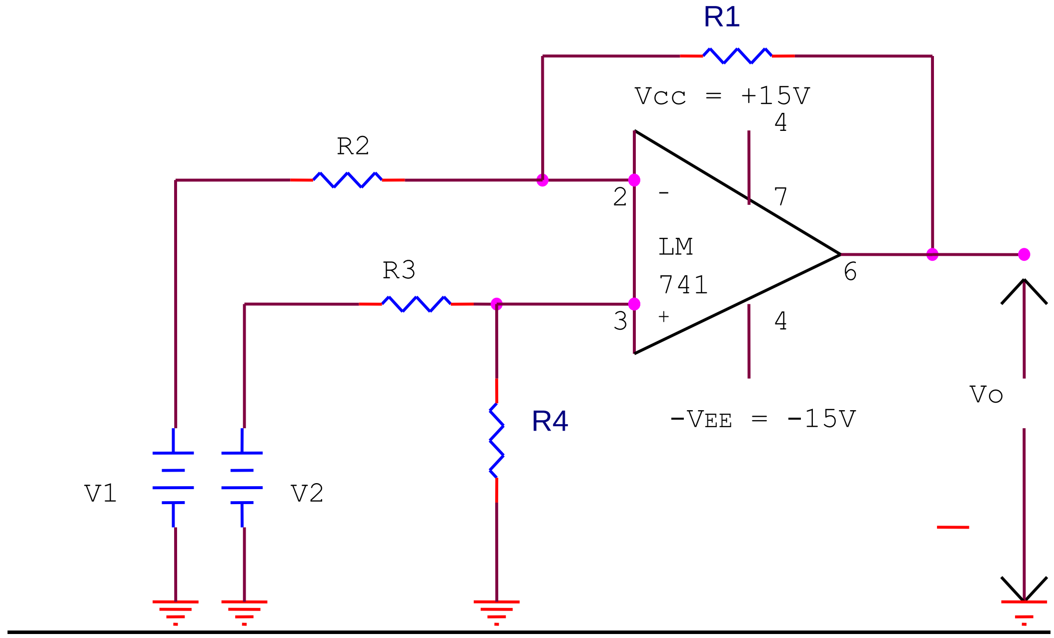
Slew Rate, SR = 2ΠfmVm /10^6 (V/μ. Sec)

b) Applications of Op – Amp:

CIRCUIT DIAGRAM: Summer: R1=R2=R3=1KΩ



Subtractor: R1=R2=R3=R4=1KΩ



Procedure:

1. Summing Amplifier:

Op amp may be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or a summer. If V1, V_2 are two input signals given to the inverting terminal, then

$$V_o = -\frac{R_F}{R}(V_1 + V_2)$$

I. Summing Amplifier:

1. Connections are made as per the circuit diagram.
2. Input voltages V_1 and V_2 are given and the corresponding output voltage V_o is measured from CRO.
3. Output varies as $V_o = -(V_1 + V_2)$, since $R_F = R$.

II. Subtracting Amplifier:

The function of a subtractor is to provide an output, which is equal to the difference of two input signals (or) proportional to the difference of two input signals. If V_1 and V_2 are the input voltages at inverting and non – inverting terminals, then

$$V_o = \frac{-R_F}{R}(V_1 - V_2)$$

II. Subtracting Amplifier:

1. Connections are made as per the circuit diagram.
2. Input voltage V_1 and V_2 are given to the inverting and non – inverting terminals respectively and corresponding output voltage is measured from CRO.
3. Output varies as $V_o = V_2 - V_1$.

PRECAUTIONS :

1. Loose and wrong connections should be avoided.
2. Readings are to be taken without parallax error.
3. The power should be turned off before making and breaking circuit connections.

Result: a) Measurement of Op – Amp Parameters: Determined the CMRR and slew rate of operational amplifier.

b) Applications of Op – Amp: Realized the Summing Amplifier and Subtracting Amplifier by using 741 Op-Amp.

VIVA:

1. What is offset current, offset voltage, slew rate, CMRR?
2. What are the ideal characteristics of op-amp?
3. Draw the pin out of LM741
4. What is inverting and non inverting amplifier?
5. What are the applications of op-amp?

<u>**EXPERIMENT NO: 2**</u>

OPERATIONAL AMPLIFIER AS INTEGRATOR AND DIFFERENTIATOR

Objective:

To realize Integrator and Differentiator by using 741 Op-Amp.

APPARATUS:

S.No	Apparatus	Type	Range	Quantity
01	Operational Amplifier	LM 741IC		01
02	Resistance		100KΩ ,10K, 15KΩ	1
03	Regulated Power supply		(0-30V)	01
04	Capacitors		0.01 µf, 330pf	01
05	Signal Generator		1MHz	01
06	CRO			01
07	Breadboard and Wires ,CRO Probes			

OP AMP As :

1. **Integrator:**

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator or the integration amplifier. Such a circuit is obtained by using a basic inverting amplifier configuration with the feedback resistor R_F replaced by a capacitor C_F. The output voltage is

Given by

$$V_o = - \frac{1}{RC} \int V_1 \, dt$$

Integrator is used in signal wave shaping circuits and in analog computers. If the input is a sine wave, the output is a cosine wave. If the input is a square wave, the output will be a triangular wave. In the practical integrator, R_F is connected across feedback capacitors C_F. This R_F limits the low frequency gain and minimizes the variation in the output voltage. The input signal will be integrated properly if the time constant

$T = R_1 C_F$ is larger than the time period T of the input signal.

2. Differentiator:

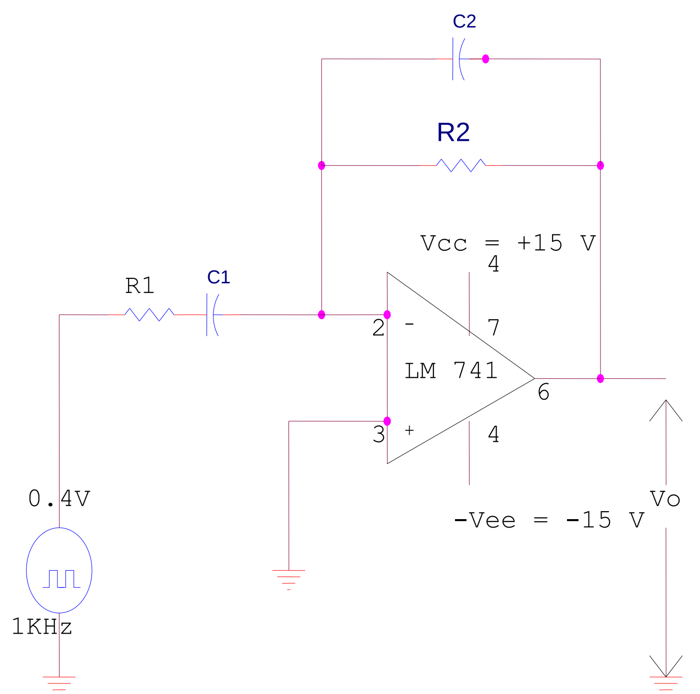
The function of a differentiator is to give an output voltage, which is proportional to the rate of change of input voltage. The differentiator may be constructed from a basic inverting amplifier if an input resistor is replaced by capacitor C_1. The output voltage is given by

$$V_o = - RC\, dV_i / dt$$

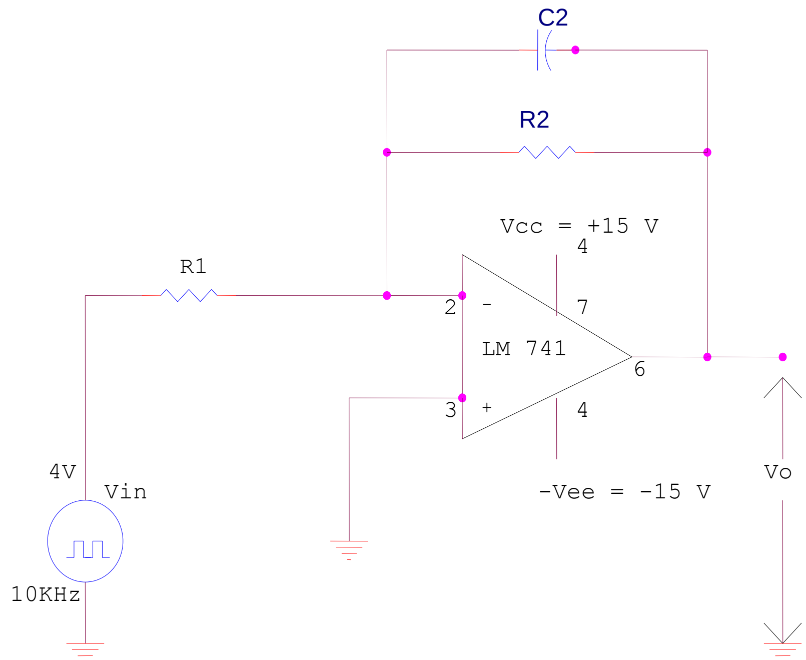
The condition for differentiator is $\tau << T$ where $\tau = C_1R_F$ for sine wave and square wave inputs, the resulting differentiated outputs are cosine wave and spike outputs respectively. Differentiator is used to detect high frequency components in an input signal.

Circuit Diagram:

Practical Differentiator: R1=10KΩ, R2=15KΩ C1=0.01µf , C2=330pf



INTEGRATOR: R1=10KΩ, R2=100KΩ, C2=0.01μf



PROCEDURE:

I. Integrator:

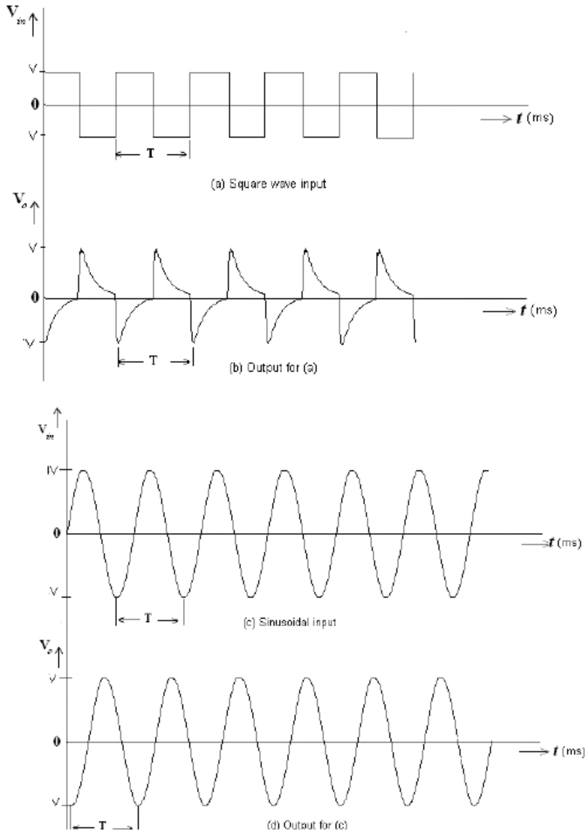
1. Connections are made as per the circuit diagram.
2. By using a function generator, a square wave input 4Vp-p is given.
3. The frequency applied is 10 KHz.
4. A perfect triangular wave is obtained. The peak-to-peak voltage and the time period of input and output waves are measured from CRO.
5. The waveforms are plotted.

II Differentiator:

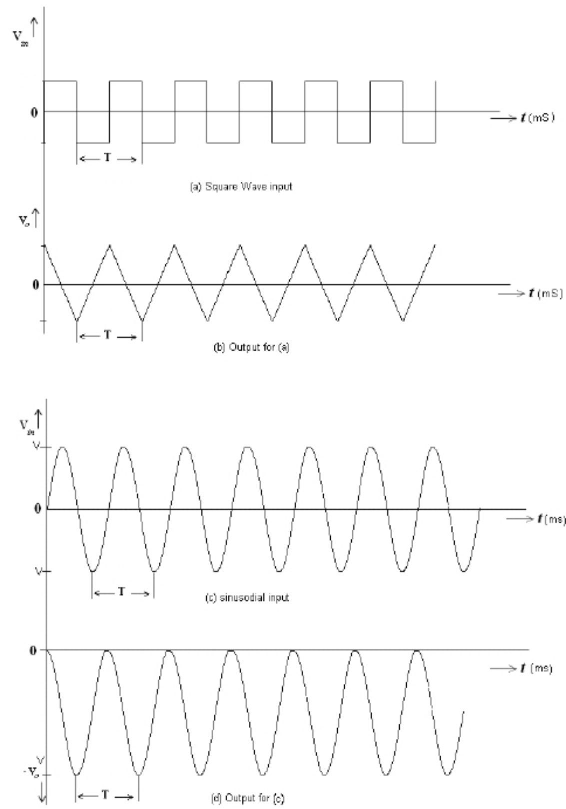
1. Connections are made as per the circuit diagram.
2. A square wave input of 4V (p-p) and frequency of 1KHZ is applied from function generator.
3. Output waveform is observed. Corresponding amplitude and time period is observed and frequency is calculated.
4. With the above data plot the output graphs with time on X-axis and voltage on Y-axis.

MODEL GRAPHS:

DIFFERENTIATOR:



INTEGRATOR:



PRECAUTIONS:

1. Loose and wrong connections are to be avoided.
2. Waveforms should be obtained without any distortion.

RESULT: Realized the Integrator and Differentiator by using 741 Op-Amp

Viva questions

1. What are the ideal characteristics of an OP-AMP?
2. Define OP-AMP.
3. What are the applications of differentiator?
4. What are the applications of integrator?
5. What is a difference between inverting and non-inverting amplifier?

EXPERIMENT NO:3

LINEAR WAVE SHAPPING

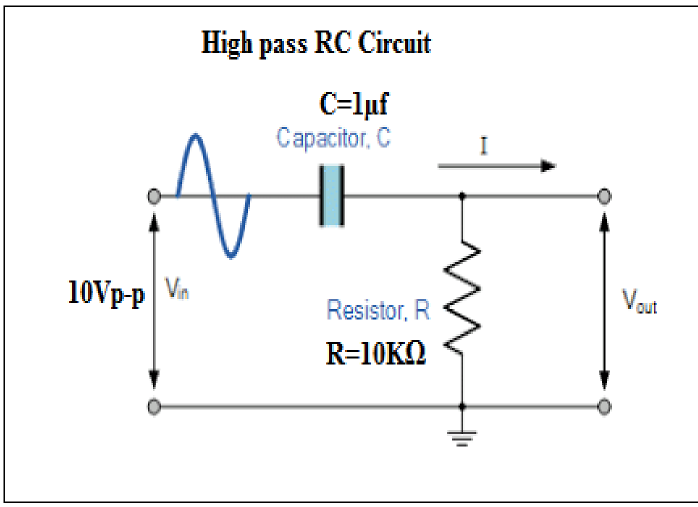
Objective:

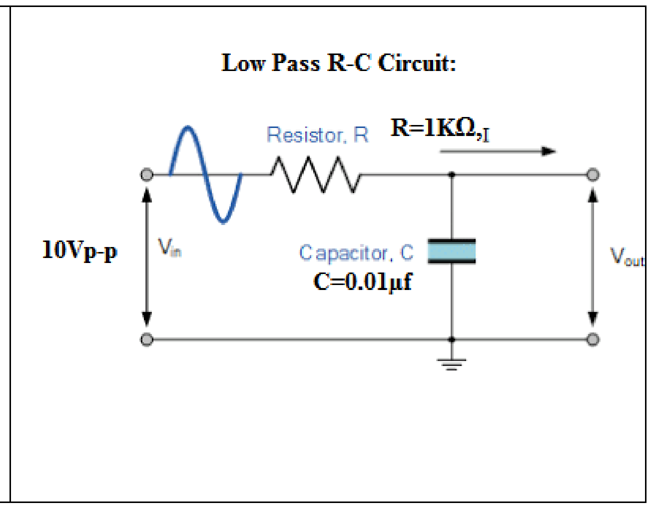
To observe the process of linear wave shaping for square wave input for high pass RC circuit and low pass RC circuit.

APPARATUS:

S.No	Apparatus	Type	Range	Quantity
1.	Resistance		1KΩ & 10KΩ	01
2.	Capacitors		0.01 µf & 0.1µf	01
3.	Regulated Power supply		(0-30V)	01
4.	Signal Generator		1MHz	01
5.	CRO			01
6.	Breadboard and Wires ,CRO Probes			

CIRCUIT DIAGRAM:





High pass RC Circuit:

The reactance of a capacitor decreases with increasing frequency; the higher frequency components in input signal appear at the output with less attenuation than do the lower frequency components. At very high frequency the capacitor acts almost as a short circuit and virtually all the input appears at the output. This behavior accounts for the designation of ‘High Pass Filter’.

Square wave responses of a high pass RC circuit.
The dashed curve represents the output if RC >> T.

$V_1^1 = V1\ exp^{(-T1/\ RC)}$ $\qquad$ $V_1^1 - V_2 = V$

$V_2^1 = V2\ exp^{(-T2/\ RC)}$ $\qquad$ $V_1 - V_2^1 = V$

A symmetrical square wave is one for which $T_1 = T_2 = T/2$. Because of symmetry $V_1 = -V_2$ and $V_1^1 = -V_2^1$

$$V_1 = V / (1+exp^{-T / 2RC})$$
$$V_1^1 = V / (1+exp^{\ T / 2RC})$$

Peaking of square wave resulting from a time constant small compared with T.

The high pass RC circuit acts as a differentiator if time constant is very small in comparisons with the time required for the input signal to make an appreciable change.

Low Pass R-C Circuit:

The low pass RC circuit passes low frequencies readily but attenuates high frequencies because the reactance of capacitor decreases with increasing frequency. At high frequencies, the capacitor acts as a virtual short circuit and output falls to zero.

Equation of rising portion V_1

$$V_1 = (Vin /2)tanhx \qquad wher\ x = T/4RC$$
$$V_1 = \text{initial value of output voltage .}$$

Equation of falling portion V_2

$$V_{02} = -V_1$$

The low pass RC circuit acts as an integrator if time constant is very large in comparison with time required for the input signal to make an appreciable change.

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. To the high pass circuit a square wave input of amplitude 10V(p-p) is given.
3. The time period of waveform is adjusted such that RC << T, RC = T and RC >>T to get spikes and tilted output respectively. The time period and amplitude are noted.
4. Now to the low pass circuit a square wave input of amplitude 10V (p-p) is given.
5. The time period of input signal is adjusted with the help of a function generator such that RC << T and RC >> T to get the corresponding waveforms. The time period and amplitude are noted.
6. Graphs are plotted for both input and output waveforms of both the circuits when RC << T and RC >> T.

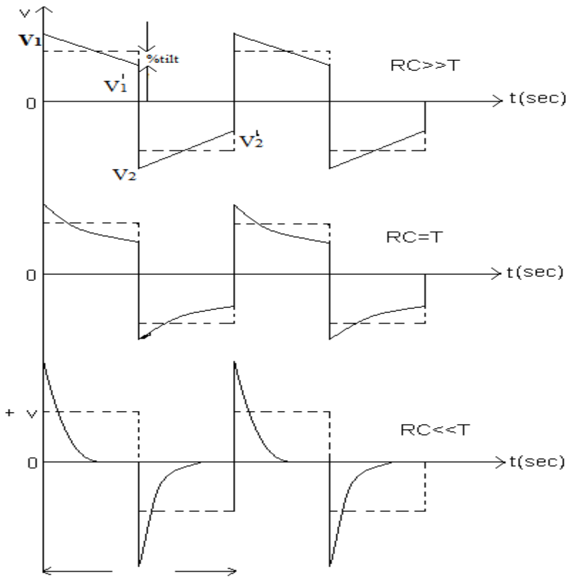
Observation Table:

	High Pass RC Circuit											
	RC >> T				RC==T				RC<<T			
Applied Frequency												
Theoretical Calculations	V_1	V'_1	V_2	V'_2	V_1	V'_1	V_2	V'_2	V_1	V'_1	V_2	V'_2
Practical Calculations												

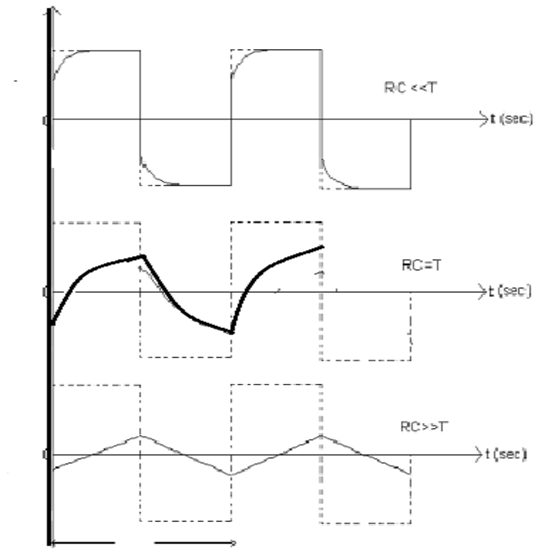
	Low Pass RC Circuit					
	RC >> T		RC==T		RC<<T	
Applied Frequency						
	V_1	V_2	V_1	V_2	V_1	V_2
Theoretical Calculations						
Practical Calculations						

MODEL GRAPHS:

High pass circuit



Low Pass Circuit



PRECAUTIONS:

1. Loose and wrong connections are to be avoided.
2. The output waveforms should be obtained without and distortion
3. Parallax error should be avoided.

RESULT: Observed the process of linear wave shaping for square wave input for high pass RC circuit and low pass RC circuit.

Viva questions

1. What is linear wave shaping
2. How low pass RC circuit works as an integrator?
3. How low pass RC circuit works as differentiator?
4. Define time constant
5. Define % tilt.
6. Explain the output wave forms of high pass and low pass circuit for different conditions.

EXPERIMENT: 4

NON- LINEAR WAVER SHAPING

a) CLIPPER CIRCUITS

Objective:

To observe the waveforms of clipper circuits using

a. Positive clipper
b. Negative clipper
c. Two level clipper or slicer circuit.

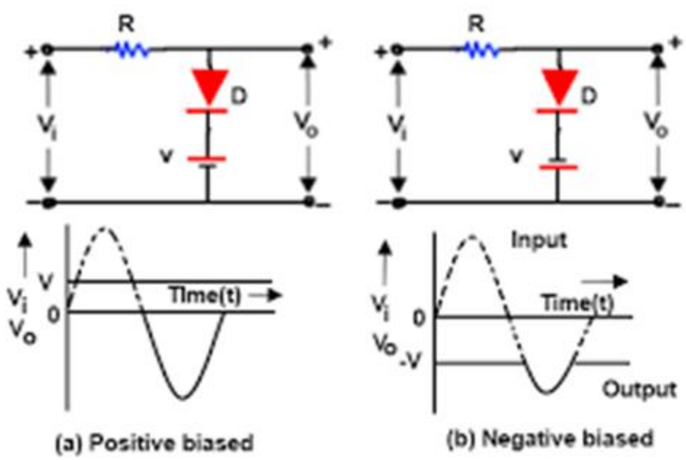
APPARATUS:

S.No	Apparatus	Type	Range	Quantity
1.	P-N diodes	1N 4007		02
2.	Resistance		10KΩ	01
3.	Regulated Power supply		(0-30V)	01
4.	Signal Generator		1MHz	01
5.	CRO			01
6.	Breadboard and Wires ,CRO Probes			

CIRCUIT DIAGRAM:

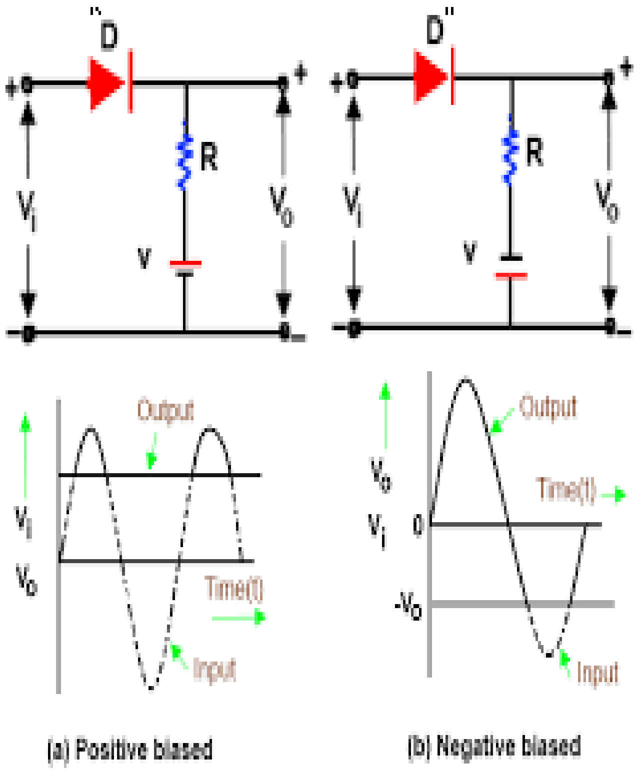
Shunt Clippers positive clipper:

R =10KΩ



Biased Shunt Positive Clipper

Series Clippers: R1=10KΩ



Biased series negative clipper

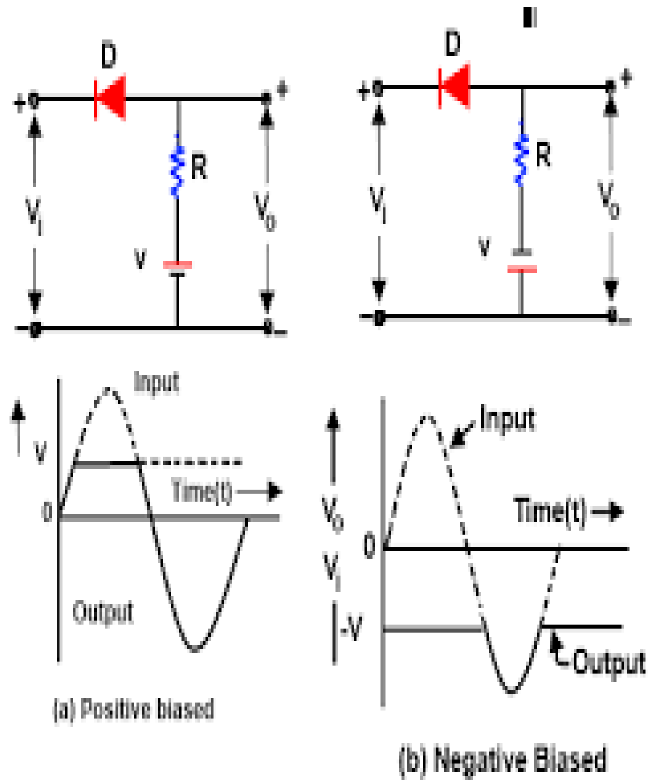
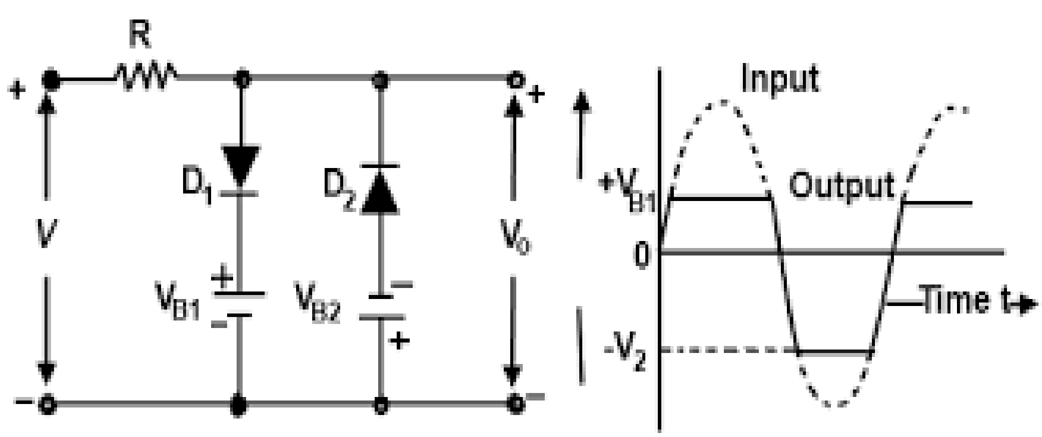


Figure 2: Series positive clipper with bias

Two level clipper: R1=10KΩ



Dual (Combination) Diode Clipper

CIRCUIT OPERATION:

Clippers are used to select a part of signal waveform above or below a reference voltage for transmission.

Negative Clipper:

For Vi < V_R +V_r , The diode D is OFF ,since it is reverse biased and hence does not contact. Since no current flows, there is no voltage drop across R.

$V_O = V_i$ for $V_i < V_R + V_r$

Where V_r is Cut-in voltage of the diode.

For $V_i > V_R + V_r$, the diode D is ON, Since it is forward biased and the potential barrier is overcome

$$V_o = V_R + V_r$$

Transfer characteristic Equation:

$V_o = V_i$ for $V_i < V_R + V_r$

$V_o = V_R + V_r$ for $V_i > V_R + V_r$

Positive Clipper:

When $V_i > V_R + V_r$ the diode is forward biased and hence it conducts since it is ON it is short circuited .It is obvious that $V_o = V_R + V_r$ Whatever the comment.

When $V_i < V_R + V_r$ the diode is reverse biased and hence it is OFF. It acts as an open Circuit. $V_o = V_i$

Transfer Characteristic Equation:

$V_o = V_i$ for $V_i < V_R + V_r$

$V_o = V_R + V_r$ for $V_i > V_R + V_r$

Procedure:

1. Connections are made as per the circuit diagram
2. For the positive clipper the diode is connected along with reference voltage as shown by applying the input and the output is observed on the C.R.O.
3. For the negative clipper the directions of diode and the reference voltage are reversed and by giving the input, the output is observed on the C.R.O.
4. For the Slicer Circuit has two Diodes along with reference voltages are connected as shown and output is observed on the C.R.O.
5. A sinusoidal input 10V (p-p) 1KHZ is given to positive clipper, negative clipper and slicer circuit and corresponding output is observed.

OBSERVATIONS:

Name Of the Clipper	Negative Clipper O/P		Output waveform
Wave Form	Positive peak	Negative peak	
Amplitude (p-p)			
Time Period			
Name Of the Clipper	Positive Clipper O/P		Output waveform
Wave Form	Positive peak	Negative peak	
Amplitude (p-p)			
Time Period			
Name Of the Clipper	2-Level Clipper O/P		Output waveform
Wave Form	Positive peak	Negative peak	
Amplitude (p-p)			
Time Period			

PRECAUTIONS:

1. Loose and wrong connections are to be avoided.
2. The output waveforms should be obtained without distortion.
3. Parallax error should be avoided

RESULT: Observed the waveforms of clipper circuits with & without reference voltage using

a. Positive clipper b. Negative clipper c. Two level clipper or slicer circuit.

Viva questions.

1. What is meant by non linear wave shaping?
2. What is clipper? What are the different types of clippers?
3. What are the different applications of clipper?
4. What is two level clipper
5. Explain the operation of positive and negative clipper?

b) **CLAMPER CIRCUITS**

Objective:

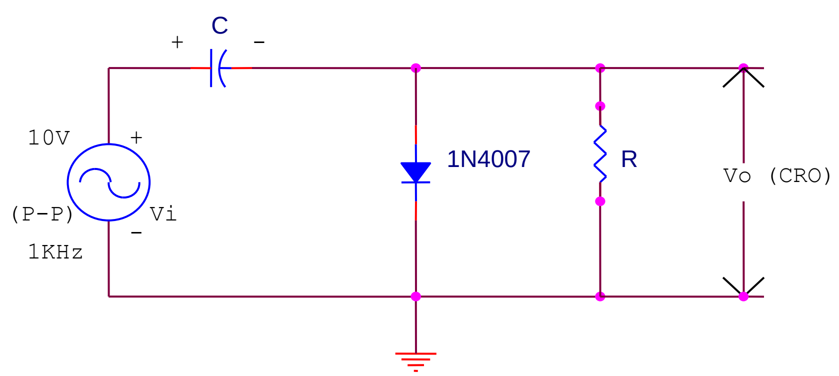
To observe the waveforms of the Positive and Negative clamping circuits.

APPARATUS:

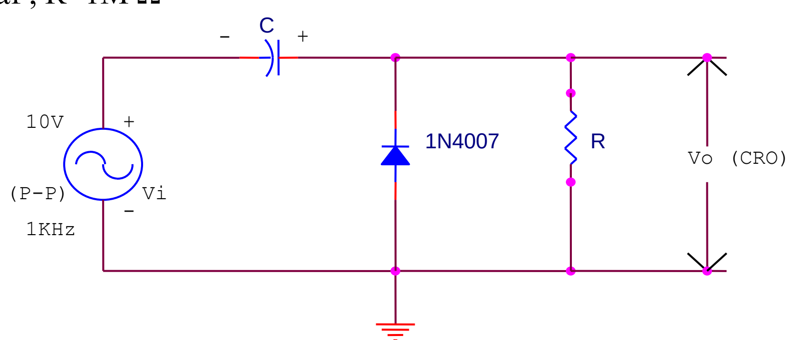
S.No	Apparatus	Type	Range	Quantity
1.	P-N diodes	1N 4007		01
2.	Resistance		1MΩ	01
3.	Capacitor		4.7µf	01
4.	Regulated Power supply		(0-30V)	01
5.	Signal Generator		1MHz	01
6.	CRO			01
7.	Breadboard and Wires ,CRO Probes			

Circuit Diagrams:

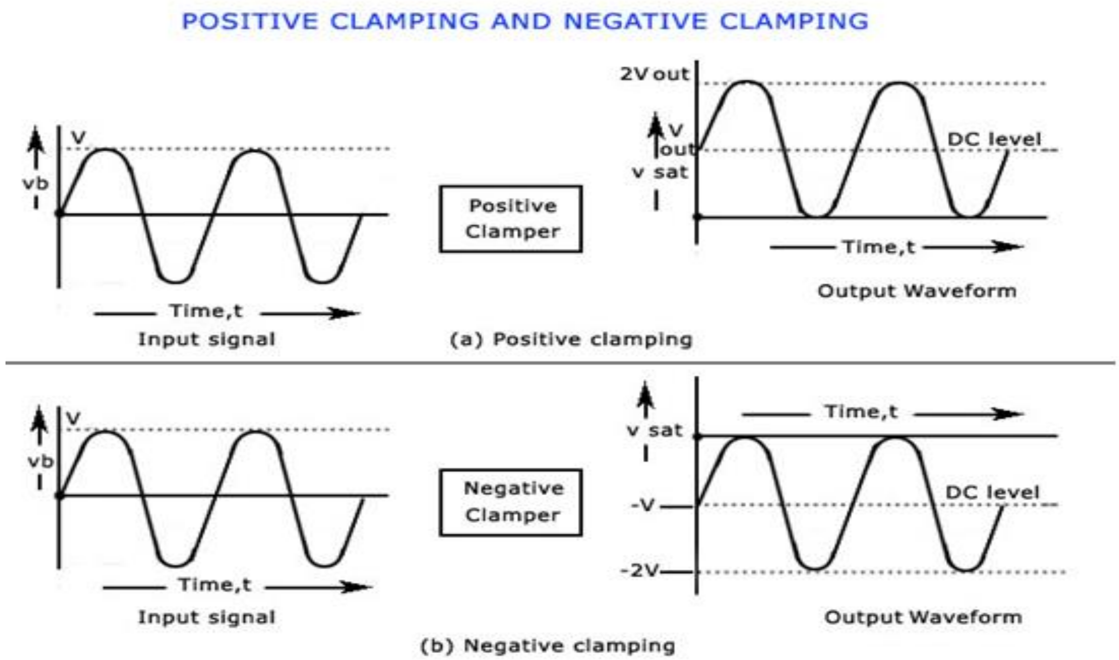
Negative Clamper: C=4.7µf , R=1M Ω



Positive Clamper: C=4.7µf , R=1M Ω



Model Graphs:



PROCEDURE:

1. The circuits are connected as per the circuit diagram.
2. The input signal Vi of (10V p-p) frequency (1KHz) is applied to each of the circuits.
3. The corresponding output waveforms are noted from the C.R.O.
4. The input and output waveform are plotted on the graph sheets.

OBSERVATIONS:

Name Of the Clamper	Negative Clamper O/P		Output waveform
Wave Form	Positive peak	Negative peak	
Amplitude (p-p)			
Time Period			

Name Of the Clamper	Positive Clamper O/P		Output waveform
Wave Form	Positive peak	Negative peak	
Amplitude (p-p)			
Time Period			

PRECAUTIONS:

1. Loose and wrong connections are to be avoided.
2. The output waveforms should be obtained without and distortion
3. Parallax error should be avoided

RESULT: Observed the waveforms of the Positive and Negative clamping circuits.

Viva questions

1. What do mean by clamper?
2. What are the different types of clamping circuits?
3. What are the different applications of clampers?
4. Why clamper is called DC inserter?
5. Explain the operation of positive clamper and negative clamper?

EXPERIMENT: 5

IC VOLTAGE REGULATOR

Objective:

To obtain the voltage regulation of a 3-terminal fixed IC voltage regulator.

Apparatus:

S.No	Apparatus	Type	Range	Quantity
1.	IC 7808			01
2.	Capacitor		1μF, 0.1 μF	01
3.	Ammeter		(0-100) mA	01
4.	Voltmeter		(0-10) V	01
5.	Regulated Power supply		(0-30V)	01
6.	Decade resistance box (DRB)			01
7.	Breadboard and Wires			

Theory:

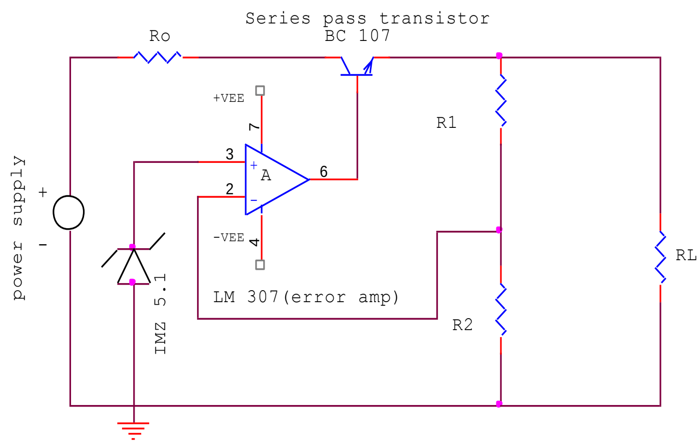
A voltage regulator is an electronic device that provides a stable dc voltage independent of load current, temperature and a.c voltage variations. Figure shows a regulated power supply using discrete components. The circuit consists of following parts.

1. Reference voltage circuit
2. Error amplifier
3. Series pass transistor
4. Feedback network.

It can be seen from the figure that the power transistor Q1 is in series with the un-regulated dc voltage V_{in} and the regulated output voltage Vo so it must absorb the difference between these two voltages whenever any fluctuation in output voltage Vo occurs

The transistor Q1 is also connected as an emitter follower and therefore provides sufficient current gain to drive the load. The output voltage is sampled by R1-R2 divider and feedback to the negative input terminal of op-amp error amplifier sample the output voltage. This sampled voltage is compared with the reference voltage V_{ref}. The output voltage Vo' of the error amplifier drives the transistor Q1.

Internal Diagram:



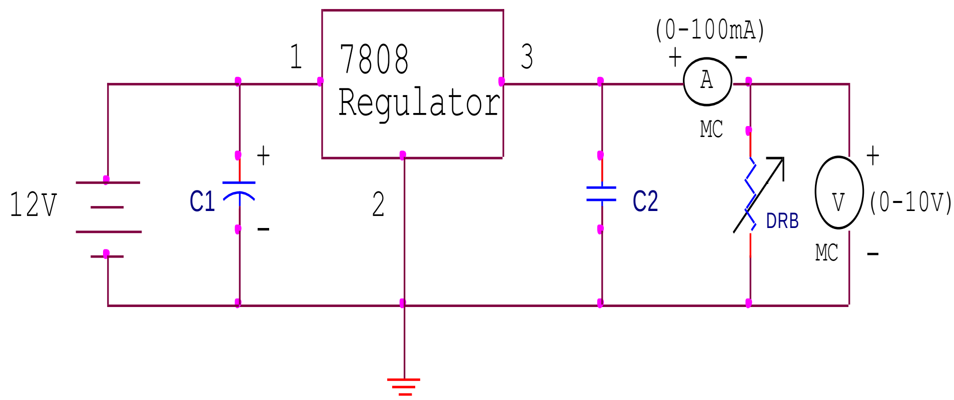
78XX series are three terminal positive fixed voltage regulators. There are seven voltage options available such as 5, 6, 8,12,15,18 and 24V. In 78XX series the last two numbers indicate the output voltage. For example 7808 indicates 8V regulator.

79 series are also 3-terminal IC regulator with fixed output negative voltage regulator.

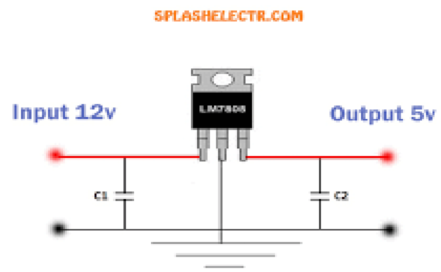
In the standard representation of monolithic voltage regulator a capacitor 'C' is usually connected between input terminal and ground to cancel the inductive effect due to long distribution leads.

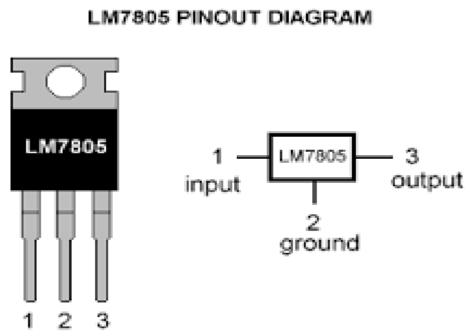
CIRCUIT DIAGRAM:

3-Terminal Fixed Voltage Regulator



C1 = 1μF , C2 = 0.1 μF





Procedure:

1. Connections are made as per the circuit diagram.
2. By adjusting the Voltage across RPS to 12V, the load terminals open circuited, the voltmeter reading is noted. This gives the no load voltage.
3. The load is varied from 10KΩ to 50Ω with the help of decade resistance box the corresponding voltmeter and ammeter reading are noted.
4. A graph is drawn between % voltage regulation on y-axis and load resistance on x-axis.

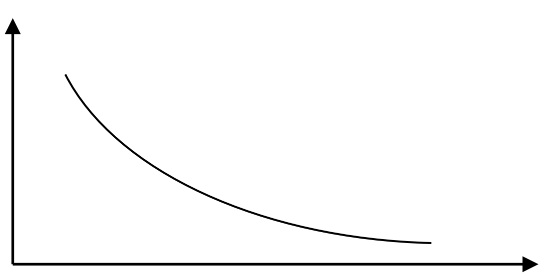
$$\% \text{ voltage Regulation} = \frac{VNL - Vl}{VL} \times 100$$

Tabular form V_{NL} =

$R_{L\ (\Omega)}$	I (mA)	V (Volts)	% Regulation
10KΩ to 50Ω			

Model Graph:

% Regulation



R in Ohms

PRECAUTIONS:

1. Loose and wrong connections are to be avoided.
2. The output waveforms should be obtained without and distortion.
3. Parallax error should be avoided

RESULT: Obtained the voltage regulation of a 3-terminal fixed IC voltage regulator

Viva questions

1. What do mean by voltage regulator?
2. What is error amplitude?
3. What is meant by error amplitude?
4. What is meant by threshold voltage?

EXPERIMENT NO: 6

SCHMITT TRIGGER

Objective:

To observe the output waveform of a Schmitt trigger circuit and to note down the hysteresis voltage V_{HY} with the reference of V_{UT} and V_{LT} .

Apparatus:

S.No	Apparatus	Type	Range	Quantity
1.	OP-AMP	IC 741		02
2.	Resistance		2.2KΩ ,10KΩ	2,1
3.	Regulated Power supply		(0-30V)	01
4.	Signal Generator		1MHz	01
5.	CRO			01
6.	Breadboard and Wires ,CRO Probes			

Theory: The circuit shown is known as the Schmitt trigger or Squaring Circuit. It shows an working comparator with positive feedback. This circuit converts an irregular shaped waveform to a square wave hence it is called as a square wave generator. If positive feedback is added to a basic comparator circuit, Gain can be increased greatly. The input voltage V_{in} triggers the output V_o every time it exceeds certain voltage levels called upper threshold voltage V_{UT} and lower threshold voltage V_{LT}

The threshold voltages are obtained by using the voltage divider R_1 - R2 where the voltage across R_1 is fed back to the (+) input. The voltage across R_1 is variable reference threshold voltage that depends on the value the polarity of the output voltage V_0 . When $V_0 = + V_{SAT}$ the voltage across R_1 is called the upper threshold Voltage $V_{UT.}$

The input voltage V_{IN} must be slightly more positive than V_{UT} in order to cause the output V_o to switch from

$+ V_{SAT}$ to $- V_{SAT}$ as long as $V_{IN} < V_{UT}$, V_O is at $+V_{SAT}$

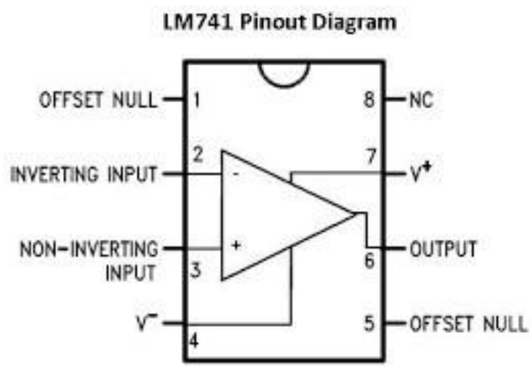
$$V_{UT} = \frac{R_2}{R_1+R_2}(+V_{SAT}) \qquad \& \; V_{LT} = \frac{R_2}{R_1+R_2}(-V_{SAT})$$

The hysteresis voltage is equal to difference between V_{UT} and V_{LT}

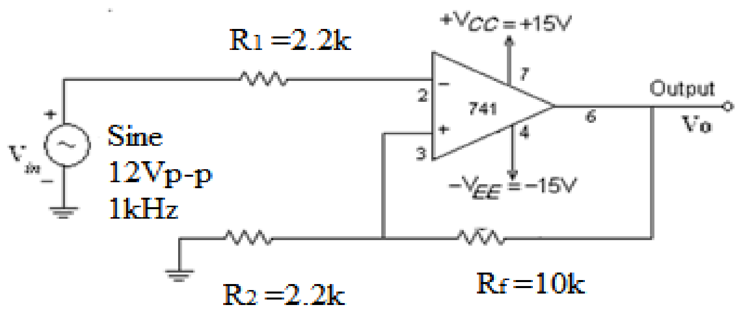
$$V_{HY} = V_{UT} - V_{LT}$$

$$V_{HY} = \frac{R_2}{R_1+R_2}(+V_{SAT}) - \frac{R_2}{R_1+R_2}(-V_{SAT})$$

Pin Diagram:

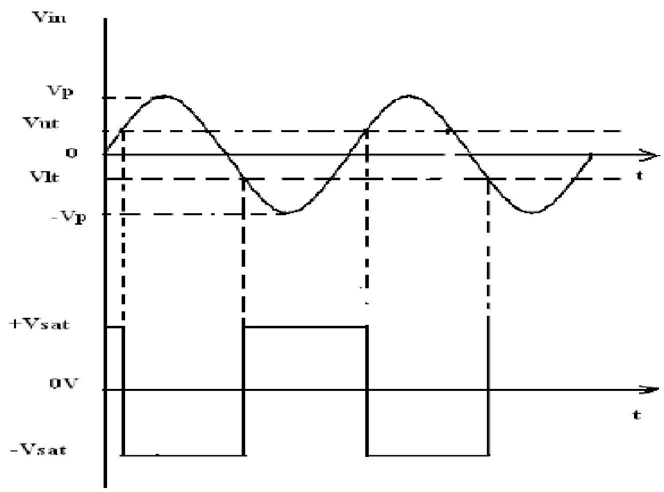


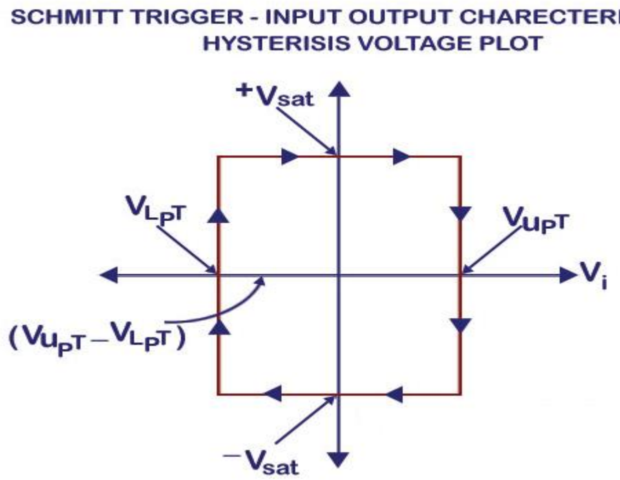
Circuit Diagram:



MODEL GRAPHS:

Input and output waveform of Schmitt trigger:





PROCEDURE:

1. The circuit for Schmitt trigger is connected as per the given circuit diagram.
2. A sinusoidal input of 1 KHz is applied with the help of function generator.
3. A square wave output is obtained for the corresponding input for which the positive peak voltage (+Vsat) and negative peak voltage (-Vsat) are noted.
4. The upper threshold voltage (V_{UT}) and lower threshold voltage (V_{LT}) are calculated for the corresponding output.
5. The shift angle (θ) is calculated using the formula

$$V_{UT} = V_p \sin\theta$$

$$\sin\theta = V_{UT} / V_p$$

$$\theta = \sin^{-1} (V_{UT} / V_p)$$

6. The hysteresis voltage (V_H) is calculated using the formula

$$V_{HY} = V_{UT} - V_{LT}$$

Observations:

Input applied: V_i (p-p mV) = , T=

Output obtained: +Vsat =

-Vsat =

T=

Calculations:

Upper threshold voltage: $V_{UT} = \frac{R_2}{R_1+R_2}(+V_{SAT})$

Lower threshold voltage:

$$V_{LT} = \frac{R_2}{R_1+R_2}(-V_{SAT})$$

Hysteresis voltage $V_{HY} = V_{UT} - V_{LT}$

Shift angle $\theta = \text{Sin}^{-1} (V_{UT}/ V_p)$

Tabular Form:

		Amplitude	Time period
Input applied	**Vi (p-p) =**		
output applied	**+Vsat=**		
	-Vsat =		

PRECAUTIONS:

1. Loose and wrong connections are to be avoided.
2. The output waveforms should be obtained without and distortion.
3. Parallax error should be avoided.

RESULT: Observed the output waveform of a Schmitt trigger circuit and noted down the hysteresis voltage V_{HY} with the reference of V_{UT} and V_{LT}.

Viva questions:

1. What do mean by Schmitt trigger?
2. What are the different applications Schmitt triggers?
3. What is meant by Hysteresis voltage?
4. What is meant by threshold voltage?

EXPERIMENT NO: 7

BISTABLE MULTIVIBRATOR

AIM: To observe the operation of fixed bias binary.

APPARATUS:

S.No	Apparatus	Type	Range	Quantity
1.	Transistors	BC 107		02
2.	Resistance		100KΩ,2.2KΩ ,15KΩ	2
3.	Regulated Power supply		(0-30V)	01
4.	Light emitting diodes			02
5.	Breadboard and Wires ,CRO Probes			

DESIGN OF A BISTABLE MULTIVIBRATOR:

For the given Vcc, V_{BB}, $h_{fe\,(min)}$, $I_{c\,(sat)}$ it is possible to compute the values of R_{c1}, R1 and R_2. The following assumptions are made in order to design the bistable fixed bias multivibrator.

1. If Q_1 and Q_2 are identical silicon transistors, the junction voltages are assumed as $V_{CE\,(sat)} = 0.3$ V and $V_{BE\,(sat)} = 0.7$ V.
2. The base current of the ON transistor is taken as 1.5 times of the minimum value of base current.
   $I_B = 1.5\, I_{B\,(min)}$
   Where $I_{B\,(min)} = I_{c\,(sat)} / h_{fe\,(min)}$
3. The current through R_2 of the ON transistor is taken as one tenth of I_C.
   If Q_2 ON, $I_4 = I_{C2}/10$.

4 The current through R_1 is ignored since it is quite small in comparison with the collector current of ON transistor.

To find R_C:

$$R_C = V_{CC} - V_D / I_2 = V_{CC} - V_{CE\,(sat)} / I_{C\,(sat)}$$

$$R_{C1} = R_{C2}$$

To find R_2:

The current though R_2 is I_4, where $I_4 = I_{C2}/10 = I_{C(sat)}/10$.

$$R_2 = [V_B - (-V_{BB})]/I_4$$

To find R_1:

The current through R_1 is I'

$I' = I_{B2} + I_4$

$I_1 = I'$

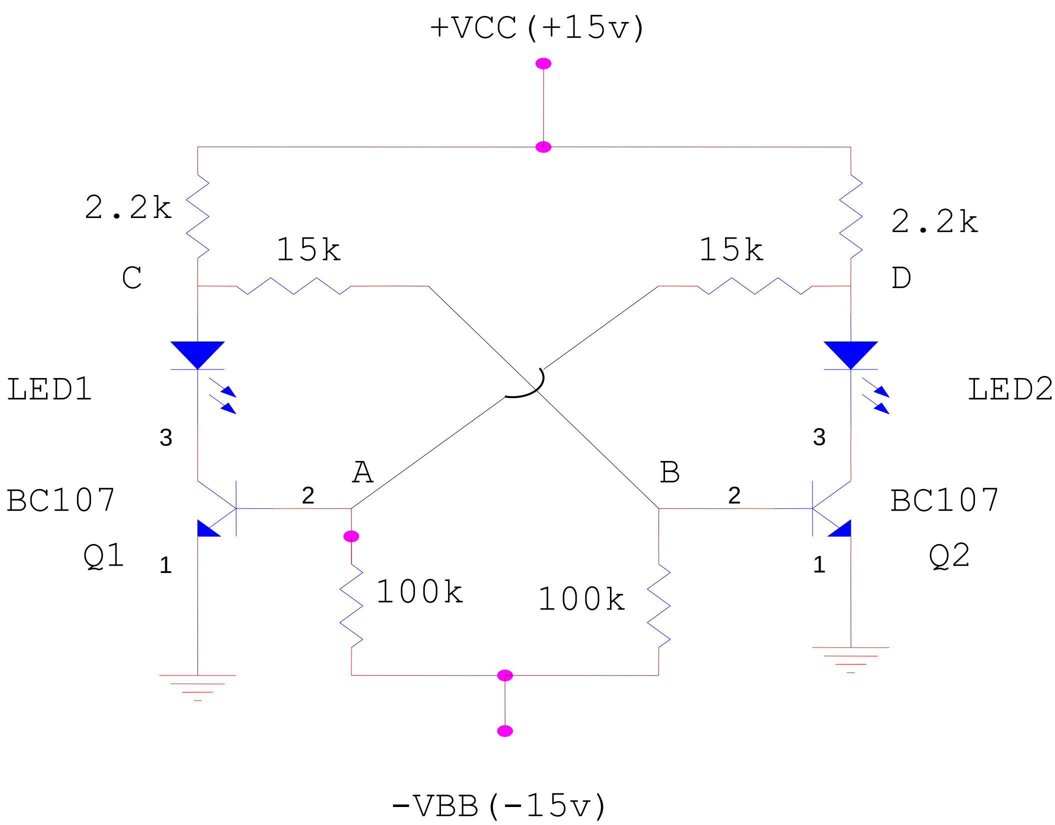
$I_{B2} = 1.5\ I_{B(min)}$

Where $I_{B(min)} = I_{C(sat)}/h_{fe(min)}$.

$I_1 = V_{CC} - V_B/R_{C1} + R_1$

$R_1 = [V_{CC} - V_{BE(SAT)}/I_1] - R_{C1}$

<u>CIRCUIT DIAGRAM</u>:



Tabular Form:

Condition 1		Condition 2	
Q1 at saturation	Q2 at cutoff	Q1 at cutoff	Q2 at saturation
V_{BE1} (sat) =	V_{BE2}(cutoff)=	V_{BE1}(cutoff)=	V_{BE2} (sat)=
V_{CE1} (sat)=	V_{CE2}(cutoff)=	V_{CE1}(cutoff)=	V_{CE2} (sat)=
V_{CB1}(sat)=	V_{CB2}(cutoff)=	V_{CB1}(cutoff)=	V_{CB2}(sat)=

PROCEDURE:

1. The connections are made as per the circuit diagram.
2. The supply is switched on and it is observed that one LED is ON whereas the other is OFF.
3. Now the base voltages of both the transistors V_{B1} and V_{B2} and collector voltages V_{C1} and V_{C2} are noted.
4. A negative trigger is given at the base of the ON transistor to change the states of the transistors.
5. In this steady state the base voltages of both the transistors V_{B1} and V_{B2} and also the collector voltages V_{C1} and V_{C2} are noted.

PRECAUTIONS:

1. Loose and wrong connections should be avoided.
2. Parallax error should be avoided.

RESULT: Observed the operation of fixed bias binary.

Viva questions

1. What is stable state?
2. Name the types of multivibrators?
3. What is quasi stable state?
4. How many stable states are there in binary?
5. What is the need of triggering
6. What are the types of triggering are there in multivibrator?

EXPERIMENT: 8

ASTABLE MULTIVIBRATOR USING 555 IC

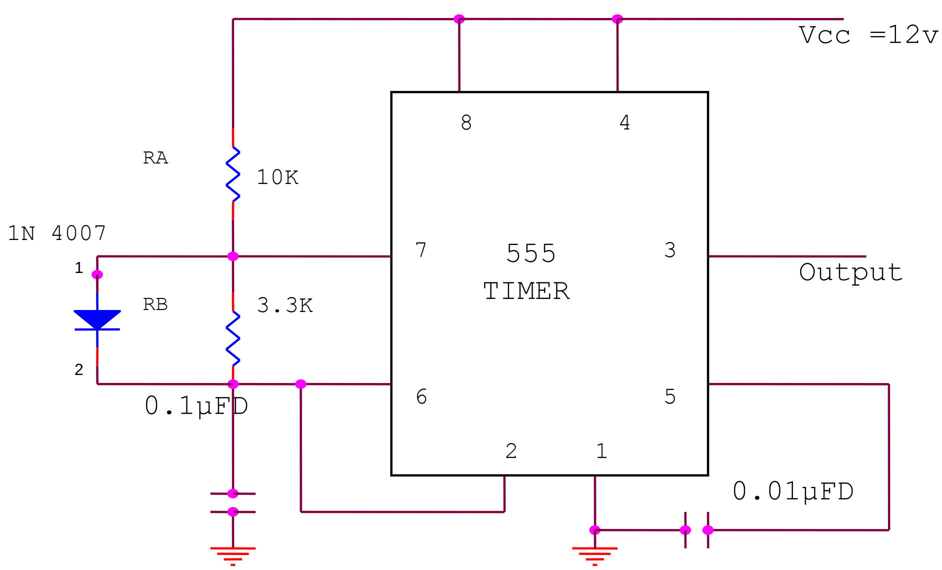
Objective:

To obtain a symmetric square wave output by maintaining certain duty cycle by using 555 IC.

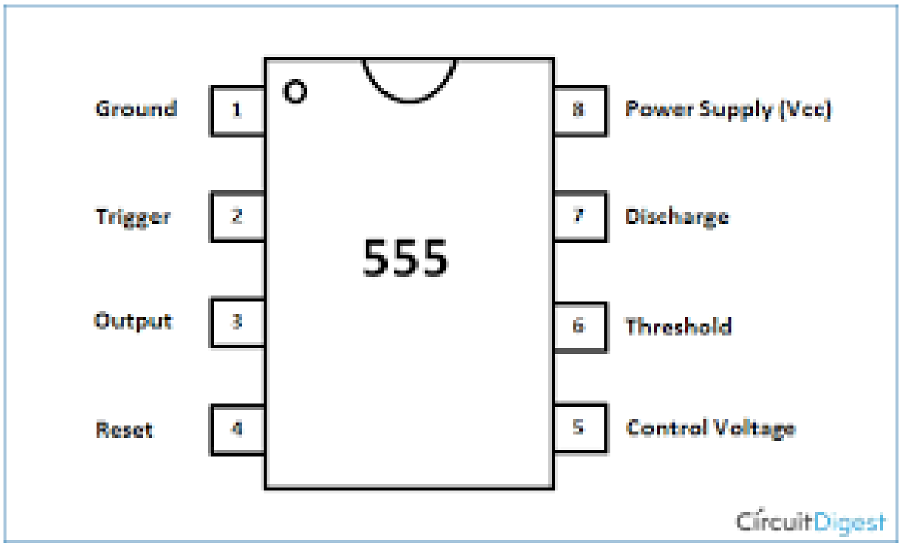
APPARATUS:

S.No	Apparatus	Type	Range	Quantity
1.	Timer	555 IC		02
2.	P N diode	1N4007		01
3.	Resistance		3.3KΩ	02
4.	Capacitors		0.1μF, 0.01μF	01
5.	Potentiometer		10KΩ	01
6.	Regulated Power supply		(0-30V)	01
7.	Breadboard and Wires ,CRO Probes			

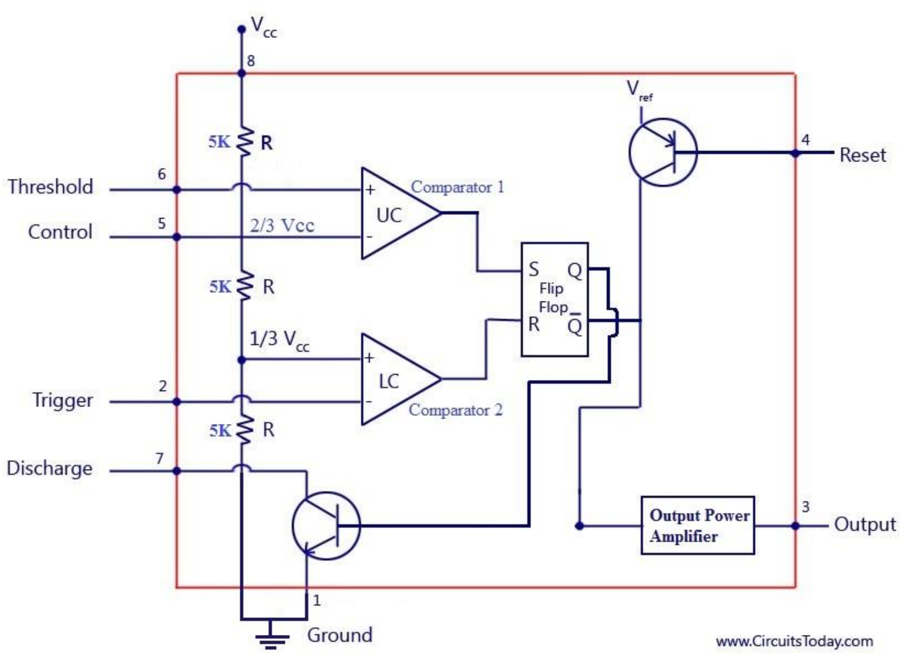
CIRCUIT DIAGRAM:



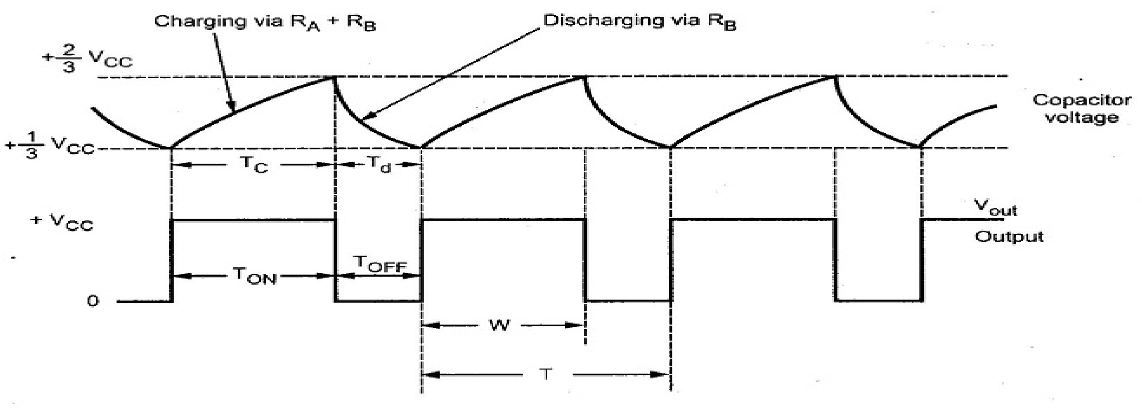
PIN DIAGRAM:



555 IC Timer Block Diagram



MODEL GRAPHS:



Waveforms of astable operation

PROCEDURE:

1. The connections are made as per the circuit diagram.
2. Now the potentiometer is adjusted till the 50% duty cycle is achieved. Output waveform is observed on the CRO.
3. Time periods of the output waveform are noted and output waveform is plotted to the scale.
4. The corresponding waveforms for other duty cycles are also obtained and plotted to scale.

Duty cycle: The capacitor voltage for a low pass RC circuit subjected to a step input of Vcc volts is given by

$$V_c = V_{cc} (1- \exp(-t/ RC))$$

The time t_1 taken by the circuit to charge from 0 to 2/3 Vcc is,

$$2/3\ V_{cc} = V_{cc} (1- \exp(-t_1/ RC))$$

$$t_1 = 1.09\ RC$$

The time t_2 to charge from 0 to 1/3 Vcc is,

$$1/3\ V_{cc} = V_{cc} (1- \exp(-t_2/ RC))$$

$$t_2 = 0.405\ RC$$

So the time to charge from 1/3 Vcc to 2/3 Vcc is

$$t_{HIGH} = t_1 - t_2 = 1.09\ RC - 0.405\ RC = 0.69\ RC$$

So, for the given circuit, $t_{HIGH} = 0.69 (R_A + R_B) C$

The output is low while the capacitor discharges from 2/3 Vcc to 1/3 Vcc and the voltage across the capacitor is given by

$$1/3\ V_{cc} = 2/3\ V_{cc}\ (\exp(-t/RC))$$

$$t_{LOW} = 0.69\ RC$$

For the given circuit, $t_{LOW} = 0.69\ R_B C$

Total time period, $T = t_{HIGH} + t_{LOW} = 0.69\ (R_A+2R_B)\ C$

Duty cycle = $t_{HIGH}/T = (R_A+R_B)/(R_A+2R_B)$

For the modified circuit Duty cycle = $R_A / (R_A+R_B)$

Tabular Form:

Duty cycle	$R_A(\Omega)$	T_{high} μ Sec	T_{low} μ Sec	Across pinNo:6		Across pin No:3	Frequency Theoretical	Frequency Practical
				V_1 (v)	V_2 (v)			

PRECAUTIONS:

1. Loose and wrong connections should be avoided.
2. Parallax error should be avoided.

RESULT: Obtained a symmetric square wave output by maintaining certain duty cycle by using 555 IC

Viva questions

1. What do mean by duty cycle?
2. What is RS flip flop?
3. What is comparator?
4. What are the applications of astable multivibrator?
5. How many stable states we have in astable multivibrator?
6. What is quasi stable state?

EXPERIMENT: 9

FREQUENCY RESPONSE OF ACTIVE FILTER

Objective:

To obtain the frequency response of active filters by varying the frequency.

APPARATUS:

S.No	Apparatus	Type	Range	Quantity
1.	OP-AMP	LM 741 IC		01
2.	Resistance		10kΩ, 16 KΩ	2,1
3.	Capacitors		0.01μF	01
4.	Function generator		1MHz	
5.	Regulated Power supply		(0-30V)	01
6.	Breadboard and Wires ,CRO Probes			

THEORY:

Filters are frequency selective networks, which can allow desired range of frequencies and attenuates other frequencies. Filters are classified:

1. Passive and Active filters

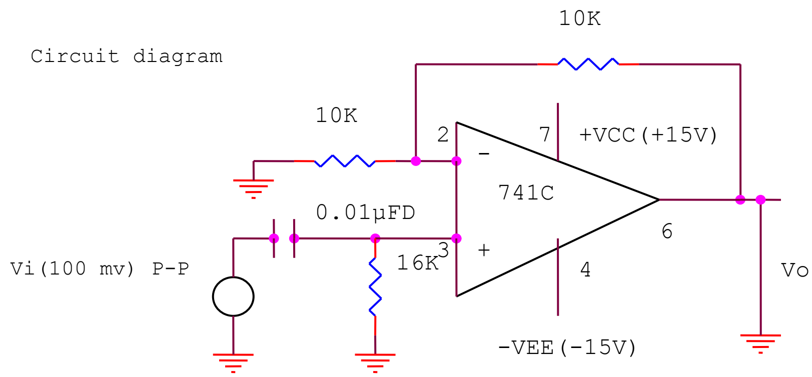
2. Analog and Digital Filters

Depending on the type of the elements used as resistor, capacitor, and inductor such a type of filter is called as passive filters. By using op-amp and transistor on addition to passive elements, they are called as active filters.

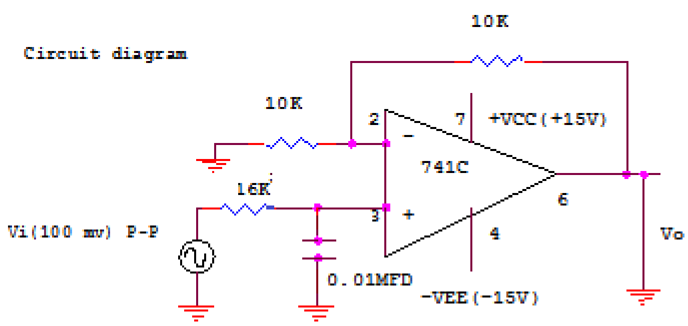
Depending on the range of frequencies the active filters can be classified as low pass, band pass, high pass, all pass, band reject filters.

CIRCUIT DIAGRAM:

HIGH PASS BUTTERWORTH FILTER

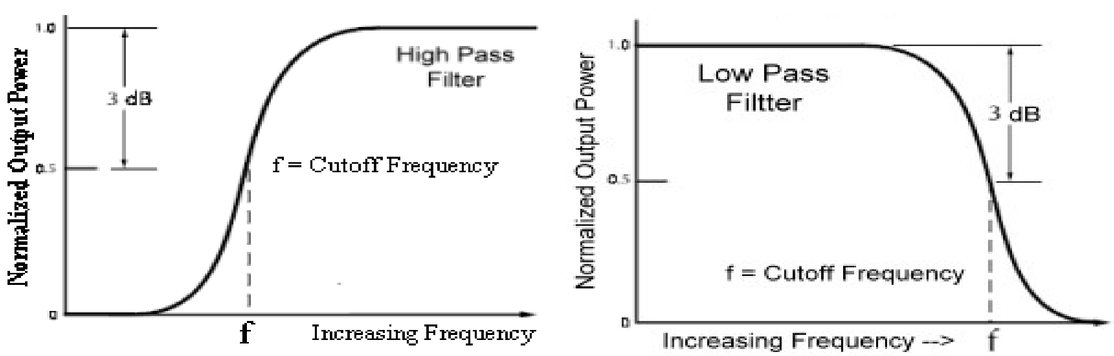


LOW PASS BUTTERWORTH FILTER



MODEL GRAPHS:

HGIH PASS BUTTERWORTH FILTER & LOW PASS BUTTERWORTH FILTER



DESIGN:

Design of I order Butter worth filter:

Given the cut off frequency F_L, A_O,

$F_L = 1/2\pi RC$

Assume C and then substituting the value in the above formula

Find R, using A_O and assuming R1 find RF

PROCEDURE:

1. The circuit is connected as per the circuit diagram
2. The Frequency of the input signal is varied and the Corresponding out put voltage is noted. The magnitude of the input Signal is kept constant through out the experiment.
3. The gain for each frequency is calculated using the formula

   Gain in dB=20 log (V_O/V_I).
4. A graph for gain v/s frequency is plotted which is known as Frequency response.

TABULAR FORM:

HIGH PASS BUTTERWORTH FILTER

Input Voltage:100 mv (p-p)

Frequency (Hz)	Out Put Voltage(V)	Gain=20log(v_0/v_i) (dB)
100Hz to 1M Hz		

LOWPASS BUTTERWORTH FILTER

Input Voltage:100 mv (p-p)

Frequency (Hz)	Out Put Voltage(V)	Gain=20log(v_0/v_i) (dB)
100Hz to 1M Hz		

PRECAUTIONS:

1. Loose and wrong connections should be avoided.
2. Parallax error should be avoided.

RESULT: Obtained the response of active filters by varying the frequency

Viva questions

1. What is filter?
2. What is an active filter?
3. What is high pass filters & low pass filters?
4. Name the types of filters?
5. What is butter worth filter?

EXPERIMENT: 10

UJT AS A RELAXATION OSCILLATOR

Objective :

To generate a ramp waveform by using UJT as a relaxation oscillator.

APPARATUS:

S.No	Apparatus	Type	Range	Quantity
1.	UJT	2N 2646		01
2.	Resistance		100Ω, 15 KΩ	2,1
3.	Capacitors		0.01µF	01
4.	Regulated Power supply		(0-30V)	01
5.	Breadboard and Wires ,CRO Probes			

ANALYSIS OF UJT:

The voltage V_{BB} is applied between B_1 and B_2. If I_E=0, then voltage drop across R_{B1} is given by,

$$V_1 = \frac{RB1}{RB1 + RB2} \times VBB$$

The ratio $\frac{RB1}{RB1+RB2}$ is termed as Intrinsic standoff ratio and is denoted by η.

$$V_1 = \eta V_{BB}$$

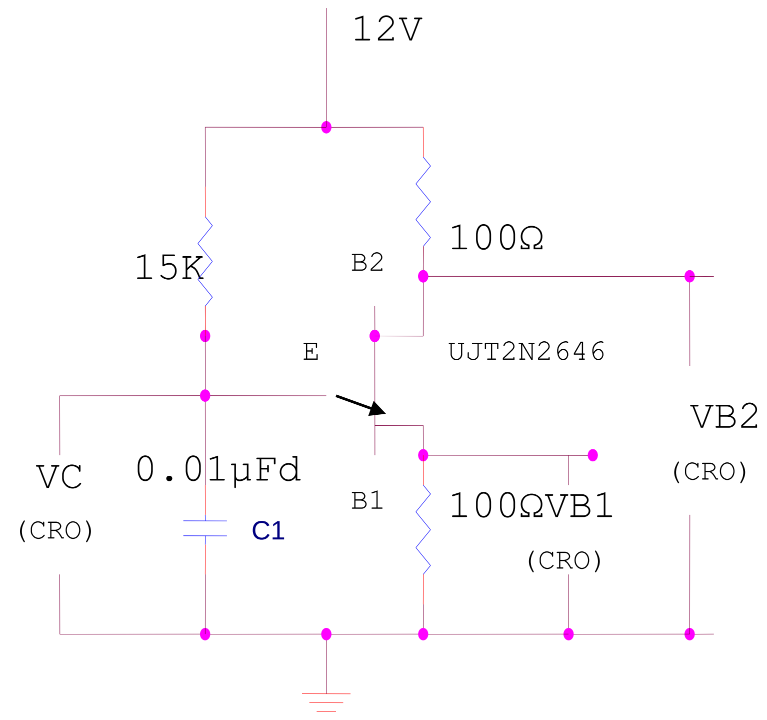
The value of emitter voltage, which makes the diode conduct, is termed as peak voltage and is given by $V_P = V_D + V_1$

$$V_P = V_D + \eta V_{BB}$$

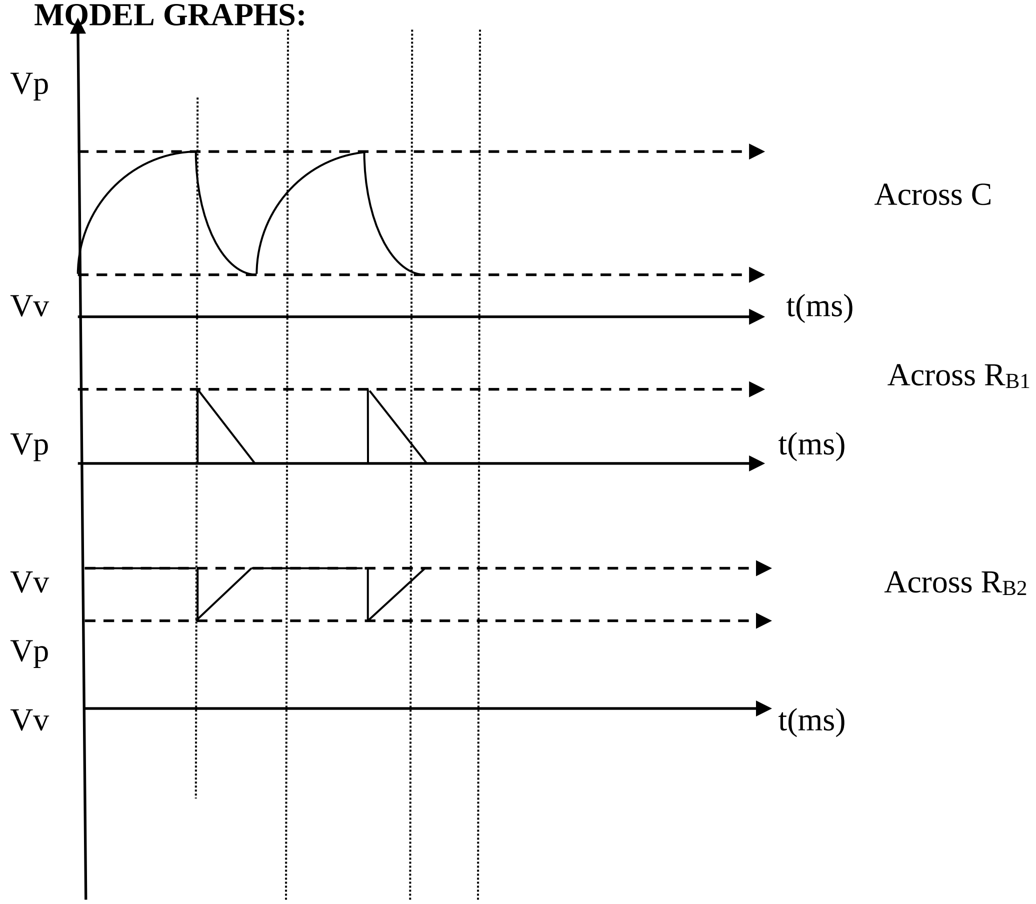
Expression for frequency of oscillation:

$$F=1/T=1/(RC\ln (1/1-\eta))$$

CIRCUIT DIAGRAM



MODEL GRAPHS:



Observation Table:

	Vv(v)	Vp(v)
Across Capacitor C		
Across Resistor R1		
Across Resistor R2		

At the capacitor:

T1----charging time period	T2 ----discharging time period	F -----frequency of oscillations F=1/T

$F=1/[RC \ln [(1/(1-\eta))]$ **$\eta = R_{B1}/(R_{B1}+R_{B2})$**

PROCEDURE:

1. The circuit is connected as per the circuit diagram.
2. A supply of V_{BB} =12v is applied to the circuit with the help of TRPS.
3. The output waveforms across capacitor, resistor R_{B1} and resistor RB2 are obtained from the CRO.
4. The frequency of the corresponding signals is noted and the waveforms are plotted on the graph sheet

PRECAUTIONS:

1) Loose and wrong connections must be avoided.
2) Parallax error should be avoided while taking the readings.

RESULT: Generated a ramp waveform by using UJT as a relaxation oscillator.

Viva questions

1. What do mean by intrinsic standoff ratio?
2. Why the wave form of RB2 is getting negative spikes?
3. What is meant by base bias resistor?

EXPERIMENT: 11

IC OP-AMP BOOT STRAP RAMP GENERATOR

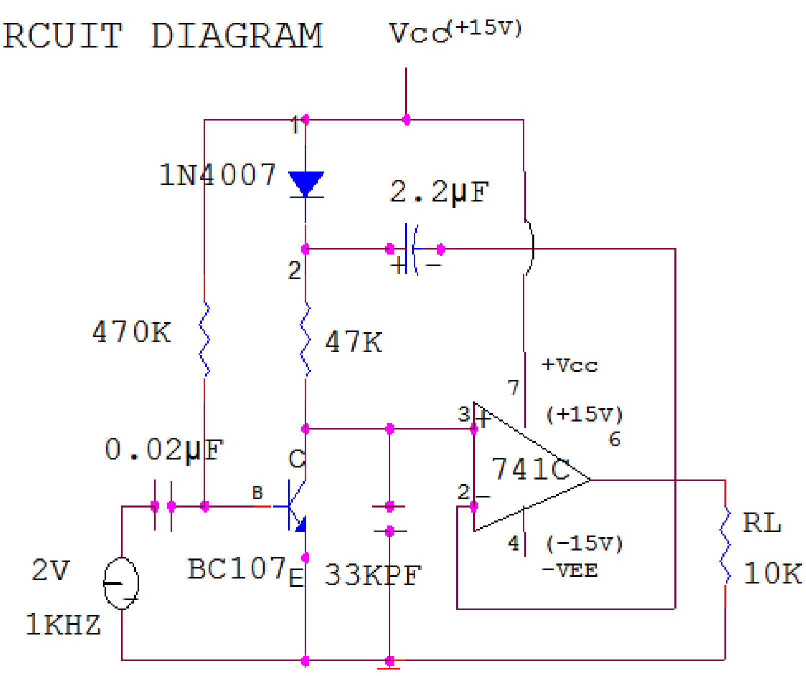
Objective:

To generate a ramp wave forms by maintaining constant current conditions by using a boot strap ramp generator with an op-amp 741 IC as voltage follower.

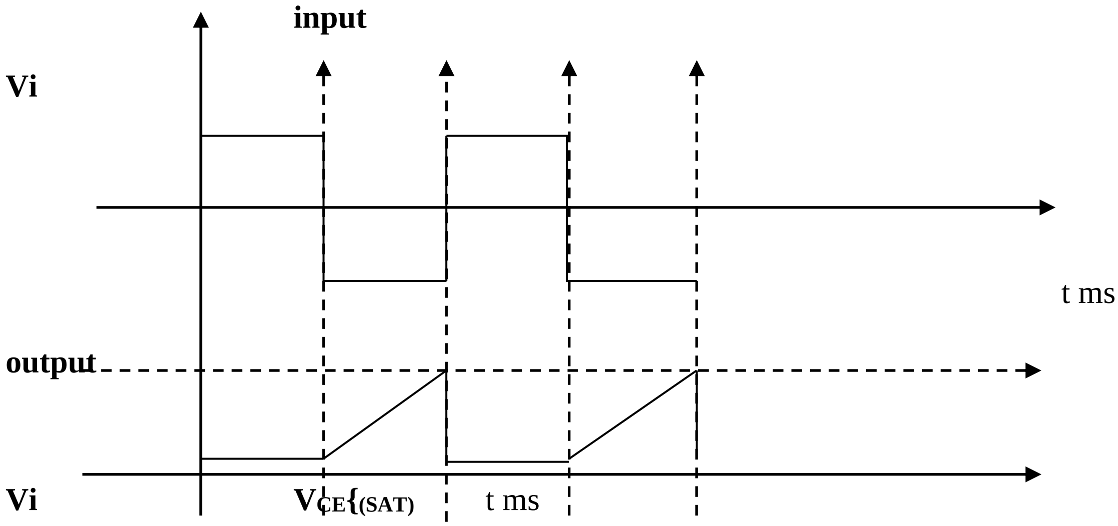
APPARATUS:

S.No	Apparatus	Type	Range	Quantity
1.	P-N Diode	1N4007		01
2.	OP-AMP	LM 741C		01
3.	Transistors	BC107		01
4.	Resistance		47kΩ, 470kΩ, 10kΩ	2,1
5.	Capacitors		33kpf,0.01µF, 2.2µF	01
6.	Regulated Power supply		(0-30V)	01
7.	Function Generator		1MHz	
8.	Breadboard and Wires ,CRO Probes			

CIRCUIT DIAGRAM



MODEL GRAPHS:



PROCEDURE:

1. The circuit is connected as per the circuit diagram.
2. A square wave of 2V (p-p), 1 KHz is applied with the help of function generator to the base of a transistor.
3. The corresponding input and output waveforms are noted from the CRO
4. The graphs are plotted for the input and output waveforms.

OBSERVATION

V_{CE} =

Output Voltage Vo =

Sweep time Ts =

PRECAUTIONS:

1. Loose and wrong connections should be avoided.
2. Parallax error should be avoided.

RESULT: Generated a ramp wave forms by maintaining constant current conditions by using a boot strap ramp generator with an op-amp 741 IC as voltage follower.

Viva questions

1. What is sweep circuit?
2. How the Op-amp acts as a emitter follower?
3. How the current constant is maintained in Boot strap?
4. Name different types of ramp generator?

EXPERIMENT: 12

Operation of R-2R ladder DAC and flash type ADC

Objective :

To study the operation of

i) R-2R DAC
ii) Flash type ADC

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1.	OP-AMP	LM 741 IC	1
2.	Resistor	1KΩ, 2KΩ	1
3.	Multimeter	-	1
4.	RPS	DUAL(0-30) V	1
5.	Breadboard and Wires ,CRO Probes Connecting Wires		

THEORY:

In weighted resistor type DAC, op-amp is used to produce a weighted sum of digital inputs where weights are produced to weights of bit positions of inputs. Each input is amplified by a factor equal to ratio of feedback resistance to input resistance to which it is connected.

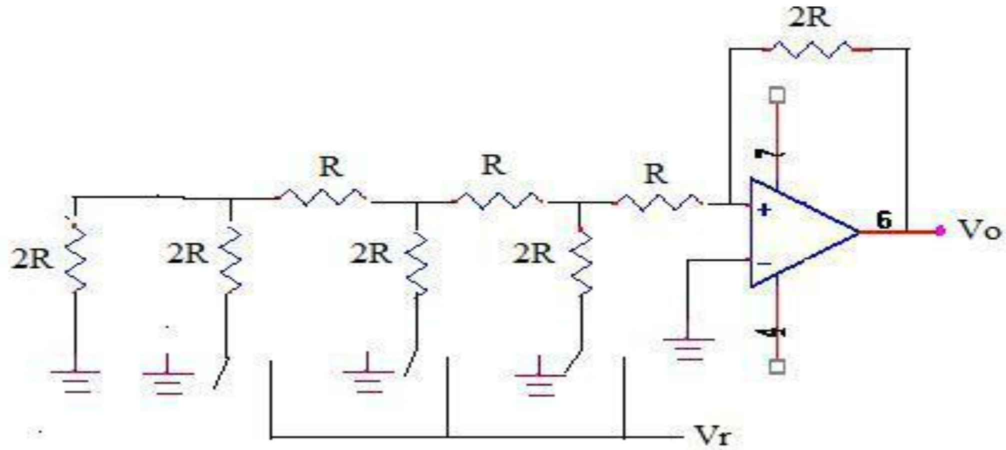
$$V_{OUT} = -R_{F/}\ /R\ \ (D_3 + 1/2\ D_2 + ¼\ D_1 + 1/8 D_0)$$

The R-2R ladder type DAC uses resistor of only two values R and2R.The inputs to resistor network may be applied through digitally connected switches or from output pins of a counter. The analogue output will be maximum, when all inputs are of logic high.

$$V = -R_f/R\ (1/2\ D_3 + 1/4 D_2 + 1/8 D_1 + 1/16 D_0)$$

In a 3 input ADC, if the analog signal exceeds the reference signal, comparator turns on. If all comparators are off, analog input will be between 0 and V/4.If C1 is high and C2 is low input will be between V/4 and V/2.If C1 andC2 are high and C3 is low input will be between 3V/4 and V.

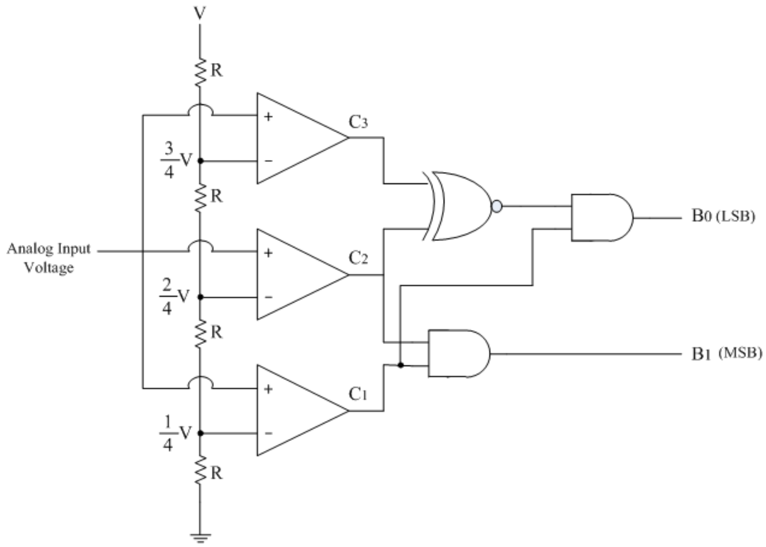
CIRCUIT DIAGRAM: **a) R-2R Ladder DAC:**



R=1KΩ Input and Output Table

S.No.	D2	D1	D0	Vth	Vprac
1)	0	0	0	0	0
2)	0	0	1	1.25	1.3
3)	0	1	0	2.5	2.7
4)	0	1	1	3.75	3.5
5)	1	0	0	5	4.9
6)	1	0	1	6.25	6.5
7)	1	1	0	7.5	7.2
8)	1	1	1	8.75	8.3

2 Bit Flash Type ADC



Input and Output Table:

Analog Input Conditions	Comparator Outputs			Digital output	
	C_1	C_2	C_3	B_1	B_0
$0 \leq V_{in} \leq \frac{V}{4}$	0	0	0	0	0
$\frac{V}{4} \leq V_{in} \leq \frac{2V}{4}$	1	0	0	0	1
$\frac{2V}{4} \leq V_{in} \leq \frac{3V}{4}$	1	1	0	1	0
$\frac{3V}{4} \leq V_{in} \leq V$	1	1	1	1	1

PROCEDURE:

1. Connect the circuit as shown in circuit diagram.
2. For various inputs, measure the outputs using multimeter.

PRECAUTIONS:

1. Loose and wrong connections should be avoided.
2. Parallax error should be avoided.

RESULT:

The operation of R-2R ladder DAC and Flash type ADC was studied

Viva Questions:

1. Which types of switches are not preferable for a simple weighted resistor DAC?
2. The inverted R-2R ladder can also be operated in?
3. What are the Multiplying DAC uses?